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A Model for Single-Event Transients in Comparators

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Abstract

A two-step modeling approach is developed for single-event transients in linear circuits that uses the PISCES device simulation program to calculate transient currents in key internal transistor structures. Those currents are then applied at the circuit level using the SPICE circuit analysis program. The results explain the dependence of transients on input differential voltage, as well as the dependence of transient signals on output loading conditions. Error rate predictions based on laboratory testing and modeling are in close agreement with the observed number of "trips" in comparators within power control modules that have operated in a deep space environment for nearly three years.

I. Introduction

Single-event transients (SETs) are produced by linear circuits when they are exposed to high-energy charged particles that deposit sufficient energy near internal p-n junctions in critical regions of the circuit. A number of papers have addressed transients in analog microcircuits [1-5], as well as in optocouplers [6,7]. Transients in differential comparators are often more important than transients in operational amplifiers because comparators usually drive digital circuits that can be triggered into an erroneous condition from a single short-duration transient, particularly if the circuit application is asynchronous. In many cases op-amps are used in applications with lower overall frequency response, or with analog feedback that can "absorb" a short-duration transient with minimal disruption. Hence, the work in this paper concentrates on transients in comparators.

As noted in all of the earlier work on linear circuits [1-4], SETs in most comparators are highly sensitive to differential input voltage (the "overdrive" condition that effectively sets the threshold of the comparator). For high values of differential input voltage, however, experimental results show that the cross section no longer depends on the differential input voltage.

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In addition to the complex dependence on input conditions more work needs to be done to determine how different load conditions and output response criteria affect output transients. Another important factor is the distribution of amplitudes and pulse widths that occur, even when a single ion is used for testing. These issues make it difficult to use experimental data taken under circuit conditions that differ from the actual application.

The purpose of the present paper is to investigate the dependence of transients in comparators in more detail, and to develop a more sophisticated modeling approach that takes the complex time dependence of internal transistor currents into account. One of the major uncertainties in developing such models is how to determine the correct value of internal currents in the various types of transistors within linear integrated circuits when they are struck with heavy ions, which result from a series of complex internal interactions. The PISCES device simulation program was used for that purpose, simulating the three basic types of internal transistors that are used in these circuits. The results of the PISCES simulations were used to determine appropriate internal current generators at the circuit level for simulations with SPICE.

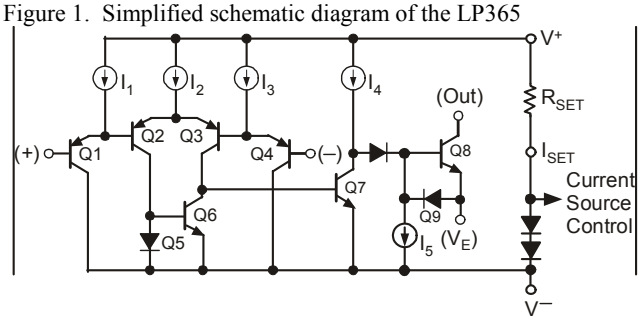
II. Experimental Approach

Transients in three types of comparators were investigated in the present study. The first was the PM139 comparator, which was also used in a hybrid power converter on the JPL Cassini spacecraft. A number of upsets have been observed in a power module that uses the PM139 during the 2 1/2-year period that Cassini has flown in deep space. More than 200 power modules are on the spacecraft, providing real space data for one particular set of application conditions. This provides an excellent opportunity to compare laboratory test data with actual space data. The PM139 devices (manufactured by Analog Devices) used in the present study were obtained from the flight lot used on the Cassini program.

The second device type was the National LP365 programmable comparator. Its design is similar to that of 139-type comparators, but it is designed to allow the operating current to be adjusted over a 50:1 range with an external control pin. The main purpose of including the LP365 in the study was to determine how changes in the first-stage operating current affect the sensitivity of the circuit to SETs.

The LM139/PM139 and LP365 circuits are very similar, except for the added feature of direct control of internal bias currents for the LP365 and the addition of steering diodes in the output circuitry of the LP365. Both circuits use a vertical (substrate) pnp transistor at the input, which is used as the first stage of a Darlington configuration. The second transistor is a lateral pnp transistor. Figure 1 shows a simplified schematic diagram of the LP365 circuit (note that R_{SET} is an *external* component). The first-stage differential transistors essentially serve as voltage-to-current converters, providing current to the second stage (transistor Q6 and diode Q5).

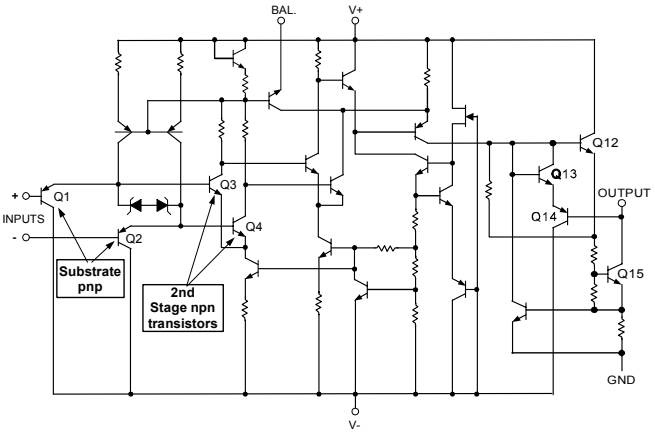
Figure 1. Simplified schematic diagram of the LP365



programmable comparator.

The third circuit type is the LM111 comparator, which is also widely used in space applications and has been the subject of several earlier radiation test studies. As shown in Figure 2, the LM111 uses a single substrate transistor, connected as an emitter follower, at the input. The output of the pair of emitter follower transistors then drives a differential npn transistor in the second stage. Although the LM111 circuit is far more complex, the initial stages denoted in Figure 2 are the critical regions of the circuit for transient responses.

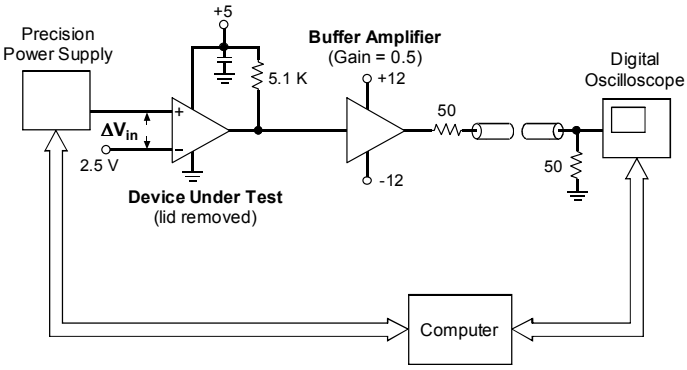
Figure 2. Schematic diagram of the LM111 comparator.



The circuits were tested with various differential input voltages, and with two different output loads, 510 and 5100 ohms. The output of the circuit was connected to a line driver to minimize capacitive loading; the line driver transmitted the output signal through a coaxial cable to a high-speed digital oscilloscope, as shown in Figure 3 (the 50-ohm series resistor at the output is used to increase the "headroom" of the line driver, and functions as a 2:1 voltage divider). The 5.1k load resistance and 5-V power supply shown in the figure are the particular circuit configuration used in the Cassini power modules. The negative supply terminal was connected to ground (an asymmetrical power supply configuration that is allowed by the normal design parameters of the 139-type comparator).

Transient waveforms from the oscilloscope were recorded on a computer for later analysis. The triggering level was set to 4.5 V (a -0.5 V transient at the output). However, because all waveforms were stored, it was possible to analyze the results for a different triggering condition after the test was completed (for example, the digital circuit driven by the comparator in the Cassini power module triggers at about 1.5 V, corresponding to a -3.5 volt transient at the comparator output).

Figure 3. Diagram of experimental configuration



Testing was done at Brookhaven National Laboratory using a number of different ions. Most of the key results were obtained for LET values below 20 MeV-cm^2/mg, where the ion range exceeds 60 µm. However, the range of ions with higher LET is considerably lower, which can affect the results for irradiations at other than normal incidence. These two circuits are fabricated on lightly doped substrates that not only have long charge collection depths, but also use collector wells that are approximately 10 µm deep (verified with spreading resistance measurements), along with a buried layer that extends even further into the substrate. This particular fabrication technology requires ions with far more range than typical digital circuits with more compact vertical structure.

III. Test Results

A. Heavy-Ion Tests of the PM139 Comparator

Cross section data for the PM139 are shown in Figure 4 for various input voltage conditions. An output voltage criterion of -0.5 V was used to trigger the oscilloscope. Typically 200 or more events were detected at each condition, leading to counting uncertainties of about 7%. Note that when the input differential voltage is below one volt the saturation cross section is nearly the same, even though the threshold LET depends strongly on input voltage. For high values of ΔV_{in} the response is quite different. The saturation cross section is nearly an order of magnitude lower than the saturation cross section for lower input voltage conditions, suggesting that different regions of the circuit are involved.

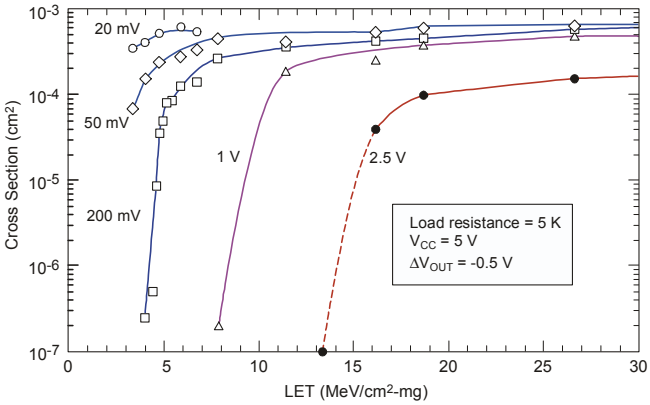


Figure 4. Cross section for the PM139 with various values of differential input voltage.

The amplitude and pulse width of the transients were also considerably different with low and high input voltages. With ΔV_{in} = 200 mV (and for lower values), the mean pulse amplitude exceeded -3 V; in other words, for ions above the threshold region nearly all of the transients had saturated amplitudes when ΔV_{in} was low. For high values of ΔV_{in} the mean output voltage depends on LET, as shown in Figure 5.

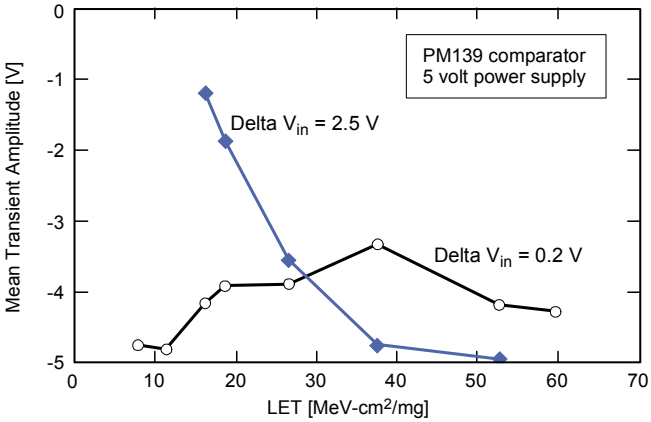


Figure 5. Pulse amplitude vs. LET for low and high input voltage.

The pulse width was also considerably different for low and high input voltage. As shown in Figure 6, the pulse width was about 0.6 µs at threshold with low ΔV_{in}. It increased to nearly 1 µs at intermediate LET values when the differential input voltage was low, and then decreased at higher LETs. For high values of ΔV_{in} the pulse width was much lower, about 0.1 µs, and was essentially independent of LET.

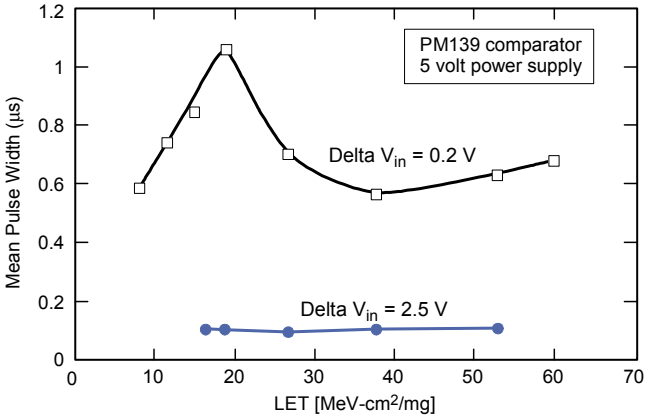


Figure 6. Pulse width vs. LET for low and high input voltage.

We also investigated the effect of changing the output triggering criterion on test results. Output triggering conditions were only important when ΔV_{in} was greater than 200 mV. Figure 7 shows how the cross section depends on the output voltage triggering condition. All of the data sets in Figure 5 used the same *input* voltage condition, ΔV_{in} = 2.5 V (which corresponds to the circuit condition in the Cassini power module); only the output trigger criterion was changed.

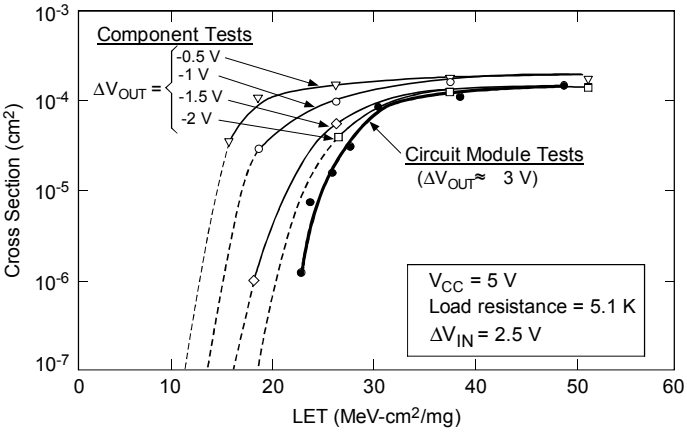


Figure 7. Dependence of cross section on output triggering voltage criteria for the PM139 comparator.

Although we do not know the output triggering conditions within the module precisely, it is approximately -3.5 V (the nominal switching threshold of the digital circuit that is driven by the comparator). Note that as ΔV_{out} increases, the cross section for tests

of individual PM139 devices is nearly identical to that measured for the circuit module.

Tests were also done with a 510-ohm load resistance to determine the effect of a different load resistance on the results (current in the output transistor depends inversely on the load resistance). If the output transistor is heavily driven into a saturated mode one would expect that the output response will have a relatively weak dependence on load conditions, but the load dependence for "weak" output transients is less apparent. The results of tests with the two load conditions are summarized in Table 1 below. The entries in the table show the ratio of the cross section for the 5.1k load to the cross section with the 510 ohm load. For low values of ΔV_{in} the cross sections are essentially the same within the limits of counting statistics, but there is a significant difference when the input voltage is high. Dashed entries correspond to conditions where the device did not upset for the particular combination of input voltage and load conditions.

Table 1
Ratio of Cross Sections for 5.1k and 510-ohm Load Conditions

ΔV_{in} (mV)	Linear Energy Transfer (MeV-cm^2/mg)		
	10	11.5	17
20	1.07	*(no data)*	0.94
50	0.95	0.98	0.96
200	1.30	1.07	1.02
1000	1.75	1.58	1.37
2500	- - -	- - -	15.2

Examining the distribution of amplitudes and pulse widths that occur with different circuit conditions provides additional insight into possible mechanisms. Key points are as follows:

<u>$\Delta V_{in} < 200$ mV</u>

(a) Nearly all transients are saturated, with a narrow distribution of amplitude and time.

(b) Results are the same for 510 and 5.1k load conditions.

(c) The threshold LET increases steadily as ΔV_{in} increases.

<u>$\Delta V_{in} > 1$ V</u>

(a) Most transients are not saturated, and there is a wide distribution in amplitude and duration.

(b) The threshold LET differs for the two load conditions, increasing as the load resistance decreases (higher output current requirement).

(c) For ΔV_{in} values above 1 V, the threshold LET makes a transition to the point where it no longer depends on the input voltage conditions.

(d) The saturation cross section becomes lower than the saturation cross section for $\Delta V_{in} < 200$ mV (about four times lower for the highest ΔV_{in} values).

Points (c) and (d) for the high input voltage condition are particularly important. The fact that the response no longer depends on input voltage suggests that the input circuitry is no longer involved in the circuit response when the differential input voltage is large. The lower cross section adds additional support to that conclusion.

B. Comparison with Earlier Work on 139-Type Devices

With low values of ΔV_{in}, both the threshold LET and the saturation cross section that we measured for the PM139 are nearly identical to the results of Koga, et al. for the National LM139 [4], even though they used a circuit with different loading conditions and power supply voltages in their tests. However, for higher values of ΔV_{in} our results are markedly different. At 1 V, our threshold LET is about 60% lower than their results, and the difference is even greater -- more than a factor of 2 -- for higher values of ΔV_{in}. Figure 8 shows the dramatic difference in our results and those of Koga, et al. for high values of ΔV_{in}. The difference can be attributed to differences in triggering criteria and loading between the two sets of experiments, which are only important for large values of differential input voltage.

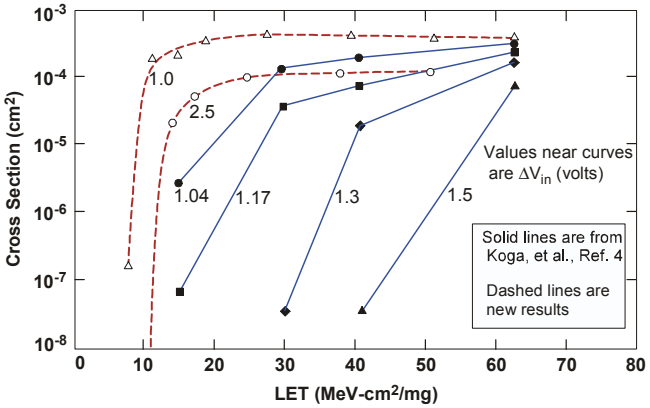


Figure 8. Comparison of cross sections for two different sets of experiments with high ΔV_{in}. Results from Ref. 4 are for the National LM139, and use a different circuit configuration than our work on the AMD PM139. Although not shown in the figure, results for low ΔV_{in} are nearly identical for the two sets of experiments.

Photomicrographs of the LM139 and PM139 show that the input transistor geometries of the two circuits are nearly identical, along with other regions of these circuits. Thus, the similarity in circuit geometries and the nearly identical results with low ΔV_{in} suggest that the response of the two types of circuits is very similar at all conditions.

C. Heavy Ion Results for LP365 Programmable Comparator

Test results for the LP365 with I_{SET} = 100 μA are shown in Figure 9. The saturation cross section at low and high values of ΔV_{in} for that device is nearly identical to those of the PM139, but the region where the threshold LET becomes independent of ΔV_{in} is more sharply defined. Reducing the programmable current lowered the threshold LET; the reduction in threshold LET was proportional to the programmable current when the device was tested with low values of ΔV_{in}.

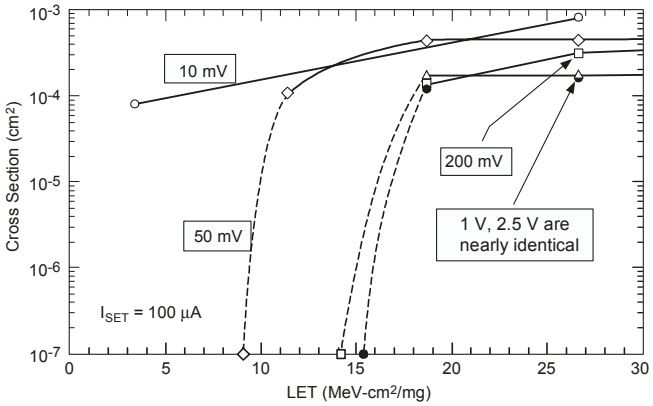


Figure 9. Cross section for the LP365 with various values of differential input voltage (programmable current set to 100 μA).

An additional set of experiments was done that involved changing the set current (reducing the current in the first stage as well as currents in other regions of the device), and investigating the effect on the cross section. Those results are shown in Figure 10. Note the sharp decrease in cross section when the current is increased beyond a critical threshold level. There is an abrupt transition from the high cross section (about 10^{-4} cm²) to the lower cross section value when the current increases beyond a critical level. Just as for the PM139, most of the transients have amplitudes near saturation when the circuit is operating in a mode where the threshold LET depends on input voltage, but the character of the response changes when the circuit operates in the mode where the response no longer depends on input conditions.

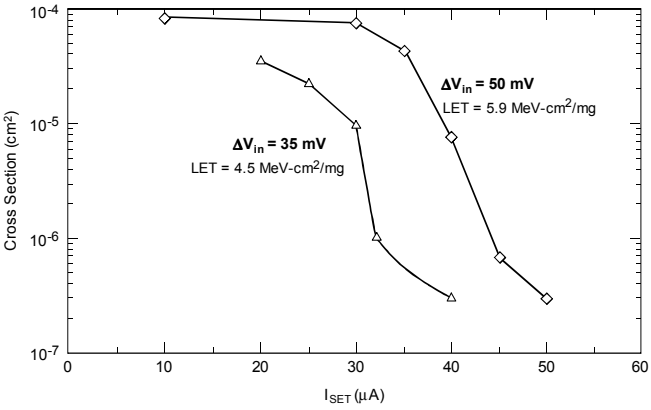


Figure 10. Dependence of cross section on set current for the LP335 programmable comparator.

D. Test Results with Californium

Tests were also done on PM139 and LP365 comparators using a ^{252}Cf fission source. Ions from the fission source have much shorter range (less than 15 μm) than heavy ions from the accelerator. However, the effective LET of the fission fragments is above 20 MeV-cm²/mg over the first 2/3 of the range, so one would clearly expect transients to be produced with californium for devices with threshold LET values below 10 MeV-cm²/mg.

Neither of the two types of comparators would produce transients when irradiated with Californium, even when ΔV was reduced to 10 mV, where the threshold LET with heavy ions is ≈ 2 MeV-cm²/mg. This null result is important in developing a model, because it demonstrates that charge collection well beyond the range of fission fragments is essential in order to produce transients in these devices. That result (which was corroborated with PISCES simulations) suggests that charge generated within the substrate region plays a dominant role in the response of these devices.

IV. PISCES Simulations of Individual Transistors

A. Transistor Types

Three basic types of transistors are used in these devices. The basic linear process was initially developed to optimize the performance of vertical npn transistors for a general class of linear circuits that operate with total power supply voltage up to 36 volts. The relatively high voltage restricts internal doping levels and requires relatively deep collector regions.

Within that process, it is possible to obtain vertical (substrate) pnp transistors and lateral pnp transistor. However, both types of pnp transistors are compromises, with relatively poor response time and somewhat lower gain compared to pnp transistors in

more sophisticated linear processes [8]. Table 2 compares some features of these devices. Note that there is a buried n+ region under the vertical npn and lateral pnp transistors, but not under the substrate pnp transistor. Because of the wide base regions, both types of pnp transistors have relatively slow response times, but the npn transistor has a relatively high gain-bandwidth product that allows it to respond much more readily to short-duration transients.

Table 2. Properties of the Three Basic Transistor Types

Device	Gain-Bandwidth Product (MHz)	Buried Layer
Vertical npn	300	yes
Substrate pnp	12	no
Lateral pnp	5	no

B. Structure Used for PISCES Simulations

Although PISCES is only capable of simulating two-dimensional structures, it is possible to obtain quasi-3D simulations by assuming cylindrical symmetry and restricting the ion strike location to the origin. This approach has been widely used in the past [9], and provides a far less costly and less time consuming approach than full 3-D simulations [10-13]. We used this geometrical simplification to model the linear transistors in this work.

The substrate pnp transistor used in the PM139 has a straightforward geometry with the emitter (base diffusion) extending over about 80% of the total collector diffusion area. The PISCES structure used for simulation is equivalent to a transistor with circular geometry with an annular ring for the contact, which is slightly different in detail than the rectangular geometry of the device. Those differences are not expected to be very important in determining how currents evolve in the structure, although the differences in contact placement have to be considered when interpreting simulation results.

The npn device is more complex. A physical diagram of the second-stage npn transistor (Q6 in Figure 1) used in the PM139 comparator is shown in Figure 11. Unlike the substrate pnp, a great deal of the npn transistor is "open" and not covered by the emitter. Thus, a PISCES simulation with a strike in the emitter will not simulate current strikes in other regions of the device. Additional simulations were done with the emitter removed from the PISCES structure as well as with both the emitter and base regions removed in order to determine how ion strikes in more remote regions of the npn transistor affect the device. This is particularly important for the npn transistor because the emitter covers such a small fractional area.

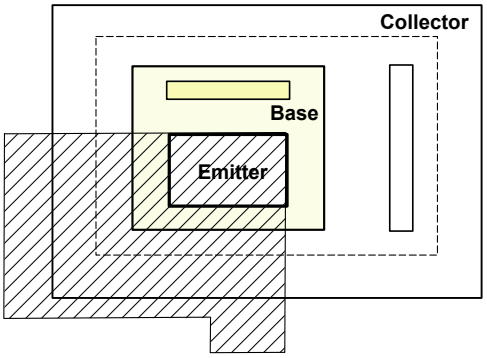


Figure 11. Physical diagram of the second-stage transistor of the PM139.

Note that the emitter of the transistor in Figure 11 is completely covered by metallization, making it impossible to generate currents within the emitter if a laser is used to study the response. The PISCES simulations show that current generated in this region has a pronounced effect on the net charge generated by heavy ions in this structure, and thus experiments with lasers cannot simulate the correct response in the npn transistor. The two types of pnp transistors used in the PM139 have a more open structure, and are more compatible with laser simulation.

The dimensions and doping levels used to develop the grid for PISCES simulations were determined from spreading resistance measurements. Figure 12 shows the underlying structure used to simulate the substrate pnp transistor (note the breaks in the scale). The substrate region extended to 400 μm, with the back contact extending laterally to 250 μm. Similar structures were used for the other two transistor types, with additional contacts and diffusions in the grid as well as the buried layer. The simulations were done for various bias conditions, varying the forward voltage (V_{BE}) from 0 to -0.06 V. These conditions correspond to *circuit*-level differential input voltages of -120 mV to 0 mV (twice as much forward voltage occurs in the circuit because of the Darlington input transistor configuration, doubling the voltage at the circuit level).

The ion strike was placed at the left axis of the structure of Figure 12. The ion strike was assumed to have a constant charge density, extending a distance of 150 μm into the device.

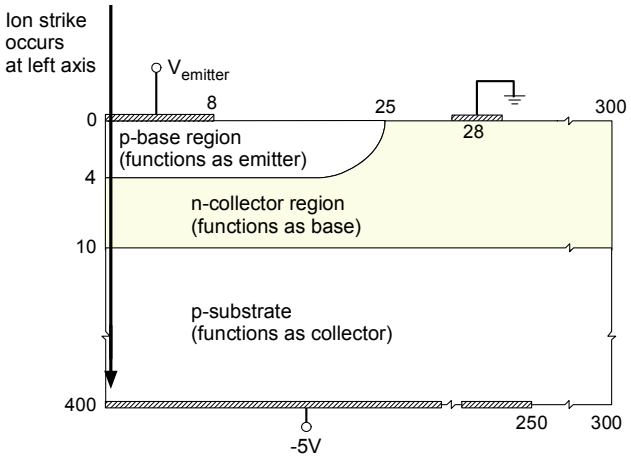


Figure 12. Structure used for PISCES simulations of the substrate pnp input transistor.

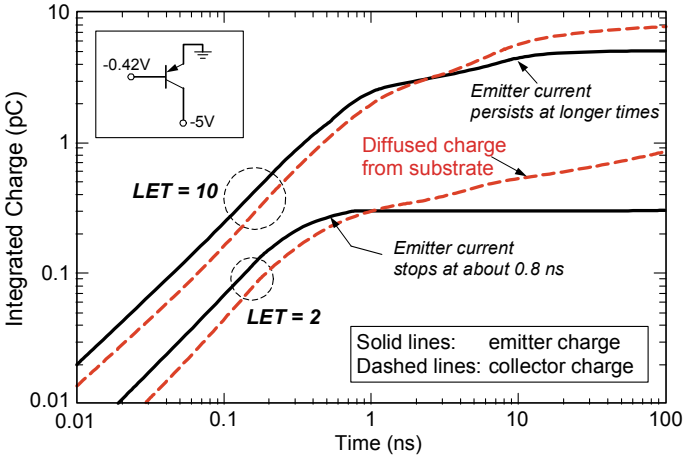


Figure 13. Integrated charge in the emitter and collector of the substrate pnp transistor for two different LET values.

C. PISCES Simulation Results for the Substrate pnp Transistor

It is not possible to cover all aspects of the PISCES simulations in a paper of this length, so detailed results will be shown only for the substrate pnp transistor. The example in Figure 13 shows the integrated charge for the condition where V_{BE} = -0.42 V (simulations were done for several different values of V_{BE}, but detailed results are shown only for one condition). V_{BE} = -0.42 corresponds to a differential input voltage of 360 mV in the PM139 circuit, with the simulated transistor weakly on. The time evolution of charge from the ion strike is shown for the emitter and collector regions. Simulation results are shown for two different equivalent ion tracks: LET = 2 MeV-cm^2/mg and LET = 10 MeV-cm^2/mg. Experimental observations showed that the lower LET value was below the threshold for circuit response with this bias condition, whereas the higher LET value was slightly above the threshold region.

The time profile of the integrated charge is shown in Figure 13. For t < 1 ns the emitter current is higher than the collector (substrate) current for both ion strike conditions. Nearly all of the current in this time regime flows through the emitter because the substrate region is collapsed by the highly localized current density caused by the ion strike. The current from the emitter splits, with some going towards the base region, and some to the substrate.

For the lower LET case, the potential in the substrate begins to recover at about 1 ns. Consequently, all current at longer times flows from the base region to the substrate, not through the emitter (*the current from the base contact changes sign when this transition occurs*). Current in the collector continues to flow at longer time because of diffused charge, primarily in the substrate.

For the higher LET case the character of the response also begins to change at about 1 ns as the internal field conditions begin to recover. However, in this case the emitter current is substantially higher at longer times, corresponding to partial turn-on of the transistor that is caused by the presence of such high charge densities at short times. At 10 ns the integrated charge in the emitter begins to flatten out, but its equilibrium value is about 16 times greater than the equilibrium charge for the lower LET condition instead of the factor of five that would be expected just from scaling the LET. Thus, the simulation clearly shows that the substrate transistor turns on for the case where LET = 10 MeV-cm^2/mg, but not for the lower LET condition.

The example shown in Figure 13 illustrates that charge collection in this structure is extremely complicated. Currents do not scale linearly with LET, even considering time periods that are too short for transistor gain to be a factor in the total charge, which was also noted in charge collection studies of diode structures by Edmonds [14]. One way to consider this is shown in Figure 14, which summarizes the results of a number of different PISCES simulations for the substrate pnp transistor. The value on the ordinate is the excess charge flowing through the collector (subtracting out charge due to the steady-state current that occurs when the bias conditions used for the simulation correspond to forward bias). For the case where V_{BE} = 0, the excess charge is nearly proportional to LET. However, as the forward voltage conditions used for the simulation are increased, the excess charge increases. With high forward bias transistor gain causes a large increase in excess charge, particularly at the higher values of LET. The gradual slope at low forward voltage conditions is mainly due

to the nonlinearity in collected charge, not transistor gain.

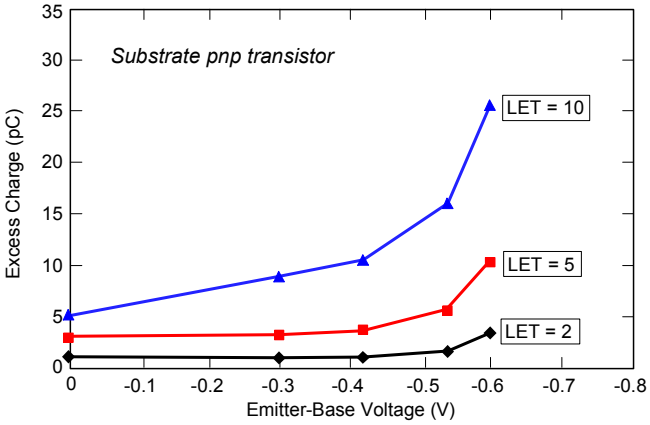


Figure 14. Dependence of excess charge in the collector on forward voltage for the substrate pnp transistor.

D. Summary of PISCES Simulation Results for the Vertical npn Transistor

The npn transistor structure is more complex than that of the substrate pnp transistor discussed in the previous subsection. Although the buried layer in the collector is effective at isolating the transistor at low injection, the PISCES results show that current at short time periods flows from the emitter to the substrate, just as for the substrate pnp transistor. This is equivalent to the so-called ion shunt effect [15]. After the internal fields recover the buried layer effectively isolates the emitter from the substrate. However, there is still a significant current in the substrate at longer time periods because of diffusion, and this current flows from the collector contact to the substrate, not from the emitter or base. Thus, there are two components to collector current. One component flows from the emitter, and the other flows to the substrate.

PISCES simulation results for the vertical npn transistor are summarized in Figure 15. Results are similar to results for the substrate pnp transistor, but transistor gain becomes important at lower forward voltage conditions. This is mainly due to the much faster response time of the npn transistor, which allows it to turn on at shorter time periods.

The excess current in Figure 15 corresponds only to current in the collector of the npn transistor. It does not include current from the collector to the substrate, which will cause some current to flow from the collector contact to the substrate. It is necessary to include that component in SPICE simulations in order to accurately simulate the overall transistor response.

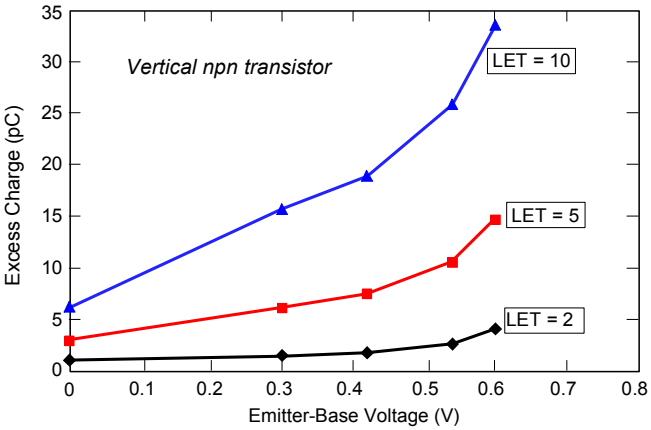


Figure 15. Dependence of excess charge in the collector on forward voltage for the vertical npn transistor.

E. Summary of PISCES Simulation Results for the Lateral pnp Transistor

The lateral pnp transistor simulation results are quite different from those of the other two types of transistors. Transistor gain is not a factor for that particular structure up to the case where LET = 20 MeV-cm^2/mg (the highest value used for PISCES simulations), even when the transistor is strongly forward biased. That is mainly due to the low gain and long response time of the lateral pnp transistor, along with the fact that much of the current generated in the base (collector diffusion) flows directly to the substrate, and does not contribute to forward biasing the lateral pnp transistor.

Figure 16 shows how charge in the emitter, base and collector evolves after an ion strike (the bias conditions are identical to those used in Figure 13 for the substrate pnp transistor). At short times the emitter current flows to the substrate, even though a buried layer is present in the structure. This occurs because the field collapses at short time intervals. After about 1 ns the internal fields begin to recover, and the emitter current begins to level off. Note that only a very small current flows into the collector region, and consequently gain amplification is not a factor for the lateral pnp until much higher LET values are reached (well above the LET values that are important for this device in the Cassini application). Note further that the charge flowing at the base terminal is much higher than that of the emitter except at short times. This current flows from the base to the substrate.

Current in the diode formed by the base region and the substrate turns out to be the major contribution for that device. Consequently, adequate SPICE simulations can be done for most lateral pnp structures by including only the substrate diode charge

contribution, ignoring transient responses in the transistor.

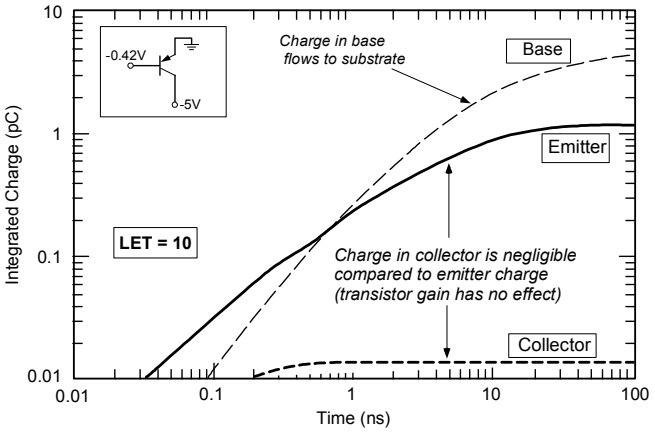


Figure 16. Charge vs. time for current components in the lateral pnp transistor.

F. Geometrical Considerations

The PISCES simulations only consider the case where the ion strike is located at the center of the emitter. The emitter of the substrate pnp transistor is only slightly smaller than that of the base region, and for that case the assumptions in the PISCES simulation are a reasonable approximation of the response of the transistor.

The npn transistor has a more complex geometry, as shown earlier in Figure 11. For that transistor the emitter area is only about 8% of that of the total transistor area (see Table 3). Thus, most ion strikes will not pass through the emitter. Those cases were simulated with the 2-D PISCES program by modifying the geometry, removing first the emitter and then the base. The result is that the npn transistor has a more sensitive region with small cross section where transistor gain adds to the total charge (corresponding to the emitter area) along with a less sensitive region that is essentially dominated by charge in the collector-substrate diode.

Table 3. Geometries of Basic Transistors in the PM139

Transistor Type	Designation in Fig. 1	Device Areas (μm^2)		
		Emitter	Base	Collector
Substrate pnp	Q1	5,100	7,780	- - -
Vertical npn	Q6	630	1,810	8,700
Lateral pnp	Q2	260	19,000	3,700

A circuit model for the npn transistor is shown in Figure 17. The two current components were determined from PISCES simulations, and the cross section is assumed to scale with the emitter and collector areas, respectively.

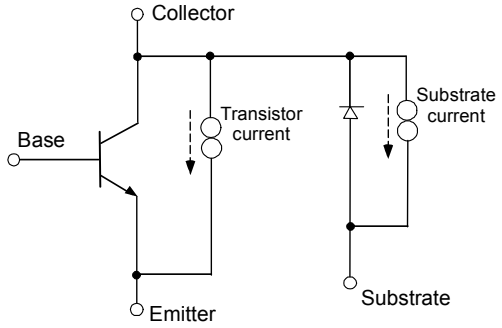


Figure 17. Currents for the vertical npn transistor for simulations with SPICE.

For the lateral pnp transistor the PISCES simulations showed that the base (collector diffusion)-substrate diode is the only significant contribution, allowing a much simpler equivalent circuit to be used.

V. Circuit Model for Transients

A. PM139 and Related Circuits

The input stage of the PM139 and LP365 consists of a basic differential input amplifier (with Darlington-connected transistors) driving a current mirror that functions as a current transfer amplifier to the second stage. For the PM139, the total emitter current of the first stage is nominally 100 μA, as shown in the simplified schematic in Figure 15. Changing ΔV_{in} essentially "steers" the fraction of the total emitter current that flows through either of the input stage transistors. Note that unless the current source itself is affected by transients, the influence of the input voltage on successive stages of the circuit only extends to the limit of current from the current source. Once the current is transferred to the opposite side of the differential transistor pair, further increase in the input voltage will no longer affect the circuit operation. Thus, with high values of ΔV_{in} the output response will effectively be decoupled from the input stage.

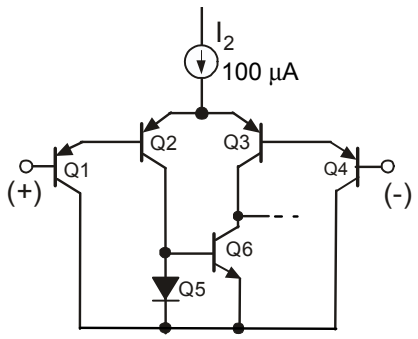


Figure 18. Simplified input schematic of the PM139/LM139 comparator.

Tests of the LP335 where current I_2 can be adjusted showed that the transition between the point where input voltage affected the output was proportional to the operating current (see Figures 9 and 10).

Input stage response mechanisms were also investigated by Koga, et al. [4]. They used a focused, pulsed laser to determine which internal regions of the circuit contributed to the response of the National LM139. They limited the laser pulse energy to 4 pJ, and thus their laser probe results only cover the lower range of LET values. We used the SPICE circuit analysis program to model the low LET region where the substrate input transistor mechanism dominates. Figure 19 compares our SPICE simulation results -- plotted here as an equivalent steady-state current during the 0.5 to 1 μs duration of the transient (see Section II) -- with the experimental results of Koga, et al. using their laser probe. The SPICE simulation only included current at the lateral pnp input transistor collector. The results agree very closely with the laser probe results. The SPICE simulation also shows that the lateral pnp transistor mechanism is not capable of producing transients with ΔV_{in} above 1 V.

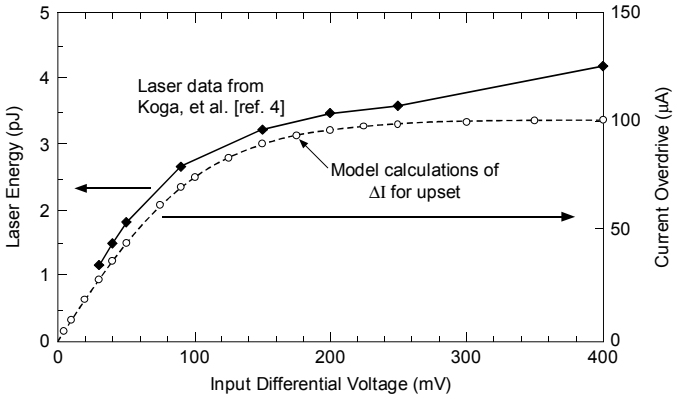


Figure 19. Comparison of SPICE model calculations with experimental laser test results from Koga, et al,. [ref. 4].

We did additional SPICE runs adding transient current to transistor Q6 (a vertical npn transistor;see Figure 1). Those runs showed the critical circuit conditions for the second response mechanism. With a large ΔV_{in} transistor Q6 is off, and the entire 100 μA from emitter current source I_2 flows from the collector of Q3 to the base of transistor Q7 (the following stage). However, substrate current in the extended region of npn transistor Q6 competes with the collector current from Q3. Once the substrate current exceeds the 100 μA value, the succeeding transistor Q7 is turned off, producing a transient at the output stage. Those results agree with our experimental observations:

(1) The response no longer depends on the input voltage.

(2) The pulse width is much shorter than the pulse width for the input transistor mechanism.

(3) The threshold depends on load resistance

(4) The saturation cross section is much smaller.

These results show that two different mechanisms are involved in the transient response of the LM139 and other basic comparator circuits that use this type of differential amplifier. The mechanism investigated by Koga, et al. [4] applies to cases where ΔV_{in} is below 0.5 V, but the second mechanism is necessary to explain how these circuits respond in applications where the differential input voltage is above one volt, such as the Cassini power module.

The saturation cross section observed experimentally for the two mechanisms agrees reasonably well with the geometrical assumptions used to determine currents from the PISCES simulations. With ΔV_{in} below 0.5 V the cross section saturates at about 6 x 10^{-4} cm^2 (see Figure 4). The total area of the lateral pnp base region is about 2.7 x 10^{-4} cm^2, with the dominant current flow from the base to the substrate. The PISCES results show that most of the charge is generated in the substrate, not the collector, so it is reasonable to increase each dimension in the rectangular structure by the diffusion length (assumed to be 50 μm), providing a total cross section of 6 x 10^{-4} cm^2 for that mechanism. That is close to the observed value for heavy ion experiments from our results as well as those obtained by Koga, et al. [4].

The mechanism in the second regime where ΔV_{in} is above 0.5 V is also dominated by collector-substrate current, but in a different internal transistor. The extended collector geometry of that device predicts a saturation cross section of approximately 1.5 x 10^{-4} cm^2 which is in close agreement with the observed results.

Some special heavy-ion experiments were done using an aperture over the PM139 that restricted the area to only that of the npn transistor that is responsible for the second mechanism. A high-power optical microscope was used to align the aperture with the location of the npn transistor (Q6 in the schematic diagram). With the aperture in place, no transients were observed at low LET. The threshold LET was about 12 MeV-cm^2/mg with the aperture in place, corroborating the modeling result about the mechanism for the case of high ΔV_{in}.

B. LM111 Comparator

Although the circuit details are different, experimental results for the LM111 comparator are quite similar to those for the PM139/LM139. Transients in the LM111 are strongly affected by ΔV_{in} for values below 1V, and less affected by ΔV_{in} for

higher values [1-4]. The saturation cross section is also about an order of magnitude lower for the case of high ΔV_{in}. However, the total cross section values are about an order of magnitude lower than of the PM139.

Although space limitations prevent a detailed discussion of modeling results, the mechanism for the response with high ΔV_{in} is turn on of the npn transistor in the first amplification stage (after the emitter follower). The saturation cross section observed experimentally is about 8 x 10^{-6} cm^2, about 20% larger than the emitter area of the npn transistor.

The SPICE analysis shows that the response for low values of ΔV_{in} is determined by emitter current in the substrate pnp transistor, which affects normally balanced currents in the substrate pnp transistors, which function as emitter followers. The LM111 exhibits a more gradual dependence on input voltage condition that the PM139/LM139 because of the emitter follower configuration at the input, which does not have the sharp cutoff conditions of the differential transistor pair used in the other circuit design.

C. Other Devices Technologies

Although we did not attempt to model comparators from other technologies, experimental work by others has shown that some types of comparators (such as the LM119) have responses that are quite different [2,4]. In particular, the SET threshold LET of those device types are not affected by the differential input voltage. Typically such devices do not use substrate or lateral pnp transistors, and operate at much higher currents with faster response times.

Charge collection in these structures will likely be quite different. Although charge in the substrate may continue to be important, the collector isolation regions are much shallower with higher doping concentrations. These devices will likely be more affected by charge in the short duration time regime where current flow can be extremely complex. Thus, developing detailed models for those devices will be a more difficult task. However, it is likely that the dominant regions in the circuit response will still be the first and second stage regions, where most of the amplification occurs.

One advantage of high-speed devices is that there are often fewer options in biasing and applying the devices. This may simplify issues relating to testing and data application, even if the internal response mechanisms are more involved. Testing and modeling such devices is an interesting area for future work.

VI. CONCLUSIONS

The work in this paper shows that transients in linear circuits are affected not only by circuit design, but also by the complex way in which charge is collected and amplified by internal transistors. Even in cases where transistor gain is not involved, the charge collection process results in net collected charge that depends in a superlinear manner on linear energy transfer that is not readily apparent from simple estimates of charge collection based on LET and charge collection depth. The collected charge at some nodes may change sign during the time period that the ion strike first distorts the internal fields and charge distribution compared to later time periods when diffused charge collection occurs. This illustrates a fundamental dilemma for circuit modeling: how to estimate the magnitude and time response of currents in internal transistors.

PISCES simulation results provide a way to solve that dilemma. Current calculated from PISCES can be applied through SPICE or other circuit analysis programs to determine circuit responses, taking internal circuit geometry into account. Although there are limitations in the quasi-3D simulation approach used with PISCES, those limitations do not appear to be very important for the linear device technology addressed in this work, which is not capable of responding to very short duration transients.

The PISCES results show that current in the diode between the isolated collector region and the substrate makes an important contribution to the charge, even for transistors with buried layers in the collector region. That contribution allows considerable simplification in establishing circuit-level models. For example, it eliminates the need to consider transistor gain in lateral pnp transistors.

SPICE simulations were done using the PISCES results to determine the correct values of charge to associate with different internal transistors within the circuit. The SPICE results are in reasonable agreement with the two different response regimes of the PM139/LM139 comparator, as determined by the different cross section and dependence on differential input voltage, and appear to be consistent with experimental observations on other types of comparators -such as the LM111 - that are fabricated with the same technology and use similar circuit design techniques. Although it is possible to combine PISCES and SPICE calculations with mixed-mode simulators [16], considerably more effort and computing capabilities are required.

There are many possible ways to design linear integrated circuits, and it will probably never be possible to develop generic approaches for the analysis of transients in linear circuits because of circuit-specific details. Nevertheless, the results of this modeling study show that the dominant contribution to single-event transient responses is due to mechanisms

associated with the first and second stages of circuits, which typically have low operating currents and high gain. This provides useful guidance in developing models as well as for simplifying analyses of more complex circuits.

Finally, note that some linear circuits are fabricated with more advanced processes that can respond much more quickly to internal transients that the relatively slow devices used in the PM139 and LM111. Those circuits are likely to be more affected by the short-duration period of charge collection, and will require more effort and sophistication for accurate modeling.

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